

LimeNET Micro 2.0

Hardware Reference Manual



Model: LimeNET Micro 2.0

Type: Indoor standalone

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Document revision: 1.0

DOCUMENT REVISION HISTORY

Version	Date	Summary of main changes
1.0	19/02/2026	Initial release
	23/032026	Final release

SAFETY GUIDELINES

Always read the technical guide before setting up or using the product. It is your responsibility to familiarise yourself with the product reference guide, other associated documentation, safety warnings, and use of the product properly and for the purpose for which it was designed.

CRITICAL SAFETY WARNINGS

- ⊖ **CRITICAL:** Never operate the unit without antennas connected to all active RF ports. Operating without proper antenna loads may cause permanent damage to the RF front-end circuitry and will void the warranty.
- ⊖ **CRITICAL:** Do not exceed the maximum safe input power of +10 dBm on any RF or GNSS connector. Exceeding this limit may cause permanent damage to the LMS7002M transceiver IC.
- ⊖ **CRITICAL:** Use only the supplied 12V DC power adapter. Using third-party or incorrectly rated adapters may damage the unit, cause overheating, or create a fire hazard.

CAUTION — POTENTIAL EQUIPMENT DAMAGE

Follow these recommendations to protect yourself and the Product from harm:

- Do not insert any sharp object into any of the Product openings.
- Do not place the Product near a heat source. Avoid placing the Product in direct sunlight.
- Do not place the Product in damp or wet environments, for example, near a bathtub, washbowl, kitchen sink or laundry tub, in a wet basement, or near a swimming pool. Do not spill any liquid on the Product.
- Do not touch the Product or its power adapter or cord with wet hands.
- Do not place the Product on an unstable surface or support.
- Do not place anything on top of the Product.
- Do not use liquid or aerosol cleaners; unplug the Product and use a soft, dry cloth for cleaning.
- When connecting a PC or other electronic devices to the Product, make sure you use the correct cable types and connect the device to the port of the Product as instructed. Incorrect links may damage the device and/or the Product.
- Do not open or attempt to open the Product. Opening or removing covers can expose you to dangerous high voltage elements or other potential risks.
- The Product contains components that emit electromagnetic waves and could interfere with pacemakers or other electronic medical devices. If you wear a pacemaker, other implantable or personal medical device, please consult your physician or medical device manufacturer for the required minimum safe distance between the Product and your medical device.
- If the Product malfunctions or fails to perform as expected, stop using it immediately.
- The Product is for indoor use only.

WARNING — RISK OF ELECTRIC SHOCK OR FIRE

- Plug in the Product power adaptor or cord to the supply voltage with correct ratings (100–240V AC, 50/60 Hz).
- Pay attention to the power load of the electrical outlet and possible extension cord. An overburdened power outlet or damaged cords and plugs may cause electric shock or fire. Check the power cords regularly. If you find any damage, replace the cord immediately.
- Do not connect the plug into an extension cord, receptacle, or other outlet unless the plug can be fully inserted with no part of the blades exposed.
- Leave adequate space for ventilation to avoid any damage caused by overheating of the Product. Do not cover the Product or its ventilation holes. Blocking these may cause fire.
- Use the power adapter provided with your Product and do not fasten the power cable to building surfaces. Ensure the cable can move freely. Do not place heavy objects on the cable.
- Do not use the Product outside, and make sure all the connections are indoors.
- Refer to the Product Summary for the standby power consumption of the device and the maximum power consumption.

REGULATORY NOTICE

⚠ WARNING: Operating RF transmitting equipment requires appropriate licensing in most jurisdictions. Users are solely responsible for ensuring compliance with all local, regional, and national radio frequency regulations. Unauthorized transmission may result in severe penalties including fines and criminal prosecution.

ENVIRONMENTAL COMPLIANCE

RoHS (Restriction of Hazardous Substances Directive): Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (2011/65/EU). The product complies with WEEE Directive for proper end-of-life disposal, EMC compliance for electromagnetic interference minimization, and CE marking for EU conformity.

The product should not be disposed of with household waste. It should be deposited in an appropriate facility to enable recovery and recycling. For more information regarding the requirements for recycling/disposal of the Product you may contact LimeNET support team.

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1 Board-Level Architecture

The LimeNET Micro 2.0 enclosure houses two primary PCB assemblies interconnected via PCIe through an M.2 HAT+ adapter. Both boards, along with their interconnects, power regulation, and thermal management components, are integrated into a custom-designed enclosure with passive convection cooling.

1.1 Baseband Board (BB) — Custom Carrier Board

The BB board is a custom carrier board designed by Lime Microsystems that hosts the Raspberry Pi 5 Compute Module. The carrier provides power regulation, connector breakout to the enclosure panels, and the critical M.2 HAT+ interface for PCIe connectivity to the SDR board (see Figure 1-1).

BB Board Component Inventory

Parameter	Specification
Compute Module	Raspberry Pi 5 CM (Broadcom BCM2712, Quad-Core Cortex-A76 @ 2.4 GHz)
SoC Architecture	ARMv8.2-A, 64-bit, Neon SIMD, Crypto extensions
Memory Subsystem	LPDDR4-4267 SDRAM with ECC (soldered to CM, 8 GB default)
Flash Storage	32 GB eMMC (soldered to CM) — boot device
PCIe Adapter	M.2 HAT+ interface for LimeSDR XTRX connection
Ethernet PHY	Gigabit (10/100/1000 auto-negotiate) with PoE receiver
Wi-Fi/BT Module	802.11 b/g/n/ac dual-band (2.4/5 GHz) + Bluetooth 5.0/BLE
USB 3.0 Hub	XHCI controller, 2× Type-A downstream ports (5 Gbps each)
USB-C Port	Alternate power delivery, CM boot/firmware update (DFU mode)
Display Outputs	2× Micro HDMI 2.0 via DSI bridge (each 4K@60 Hz, CEC)
Audio	3.5mm TRRS jack (stereo out + mono mic, CTIA)
SD Card	Micro-SD push-push socket (SDHC/SDXC, UHS-I, up to 128 GB)
GPIO Breakout	40-pin RPi header, 3.3 V logic, I2C/SPI/UART/PWM exposed
Power Input Stage	12V DC barrel (5.5 × 2.1 mm) with reverse polarity and OCP
Voltage Regulation	Step-down converters: 12 V → 5 V (main rail), 5 V → 3.3 V, 5 V → 1.8 V

Board design files are available as open-source hardware from Lime Microsystems. Full schematics, BOM, and Gerber files can be obtained from the GitHub repository or by contacting the engineering team.

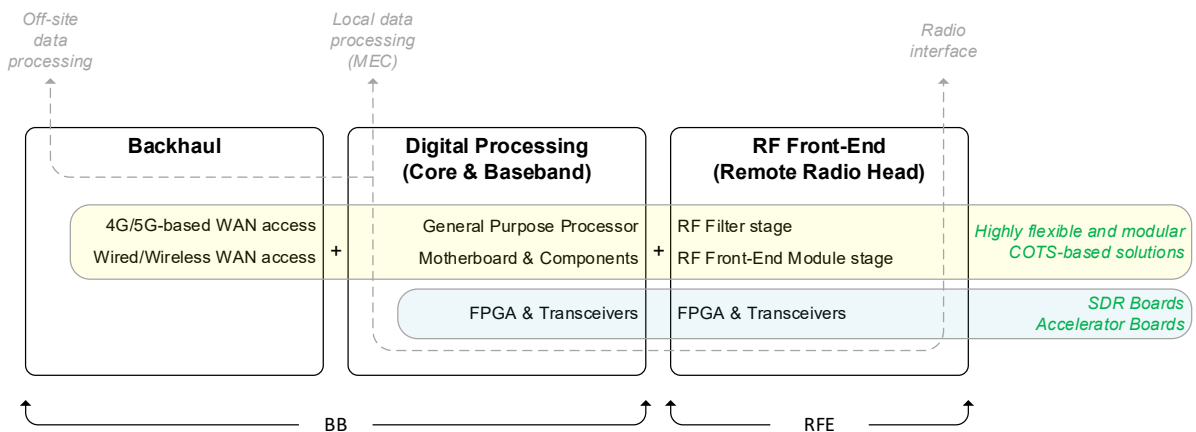


Figure 1-1: System architecture showing Backhaul, Digital Processing (BB), and RF Front-End (RFE) subsystems with COTS-based modular design.

1.2 Radio Front-End Board (RFE) — LimeSDR XTRX v1.3

The RFE board is the LimeSDR XTRX revision 1.3, a compact mini PCIe form factor SDR board that plugs into the carrier board's M.2 slot via a mechanical adapter (see Figure 1-2). It provides the complete RF signal chain and digital front-end processing.

RFE Board Component Inventory

Parameter	Specification
RF Transceiver IC	Lime Microsystems LMS7002M FPRF (QFN package)
FPGA	Xilinx Artix-7 XC7A50T-2CPG236I
FPGA Logic Cells	52,160
FPGA Block RAM	2,700 Kbits (3,600 Kbits including distributed)
FPGA DSP48E1 Slices	120 (multiply-accumulate units for DSP)
Clock Oscillators	VCOCXO + VCTCXO (± 0.2 ppm) + CDCM6208 distribution
GNSS Receiver	Multi-constellation (GPS/GLONASS/Galileo/BeiDou)
PCIe Interface	Gen2 $\times 1$ lane (5 GT/s) + high-speed SerDes
SPI Interface	Configuration bus for LMS7002M register access
RF Ports	4 \times SMA Female (TRXA, RXA, TRXB, RXB) — 50 Ω matched
GNSS Port	1 \times SMA Female (INT EXT2)
EXT SYNC Port	1 \times SMA Female (external clock reference input)
Board Dimensions	Mini PCIe expansion card form factor
Power Supply	Fed from carrier board via M.2 connector (3.3 V, 1.8 V rails)

Complete hardware documentation: github.com/myriadrf/LimeSDR-XTRX. FPGA gateway source: github.com/myriadrf/LimeSDR-XTRX_GW.

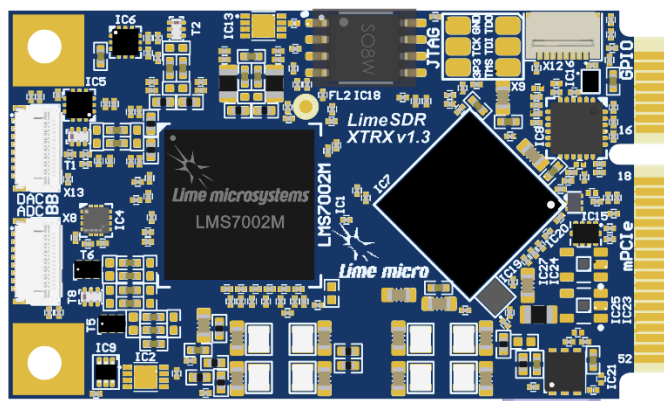


Figure 1-2: LimeSDR XTRX v1.3 RFE board — LMS7002M FPRF transceiver (center-left), Xilinx Artix-7 FPGA (center-right), clock oscillators, GNSS receiver, and mPCIe edge connector.

2 Schematics and Design Resources

LimeNET Micro follows an open-hardware philosophy. Design files for both the carrier board and the LimeSDR XTRX are available for engineers requiring board-level detail.

2.1 Design File Availability

Resource	Format	Access
Carrier Board Schematic	PDF/OrCAD	Open-source — GitHub or contact Lime engineering
Carrier Board Layout	Gerber/ODB++	Available on request
Carrier Board BOM	CSV/Excel	Available on request
LimeSDR XTRX Schematic	PDF/KiCad	Published: github.com/myriadrf/LimeSDR-XTRX
XTRX Layout/Gerber	KiCad/Gerber	Published: github.com/myriadrf/LimeSDR-XTRX
XTRX Gateware (FPGA)	Verilog/VHDL	Open-source: github.com/myriadrf/LimeSDR-XTRX_GW
LMS7002M Datasheet	PDF	limemicro.com (full register map, electrical specs)
LMS7002M Programming Guide	PDF	limemicro.com (SPI register reference)
Artix-7 Datasheet	PDF	xilinx.com/amd.com (DC, AC specs, package pinout)
BCM2712 Datasheet	PDF	Raspberry Pi Foundation (limited public release)
RPI5 CM Datasheet	PDF	datasheets.raspberrypi.com

Note: When ordering LimeNET Micro, different internal hardware configurations can be selected. The delivered unit may differ from default specifications. All custom configurations can be documented with specific schematics.

3 Supported Configurations and Operational Modes

The LimeNET Micro supports multiple radio access technologies and deployment configurations, selectable through software configuration and service scripts.

Operational Mode Reference

Mode	Duplex	Description and Requirements
5G SA TDD	TDD	Default. 5G NR Standalone (Band 38). Single cell, single carrier. 1 unit
5G SA FDD	FDD	5G NR Standalone on FDD band (e.g., Band 7). Max 10 MHz BW. 1 unit
4G LTE TDD	TDD	LTE single cell TDD mode (Band 38). 1 unit
4G LTE FDD	FDD	LTE single cell FDD mode (Band 7). Max 10 MHz BW. 1 unit
5G NSA	Mixed	Non-Standalone: 5G NR with 4G LTE anchor. Requires 2+ units minimum
Multi-Cell 5G	TDD/FDD	Multi-carrier or multi-sector 5G. Scalable, requires N units
Multi-Cell 4G	TDD/FDD	Multi-carrier or multi-sector 4G. Scalable, requires N units
5G + 4G Independent	Mixed	Concurrent separate 4G and 5G networks. 2+ units
Distributed RRH	Any	Remote Radio Head with centralized BB. N units
SISO 1×1	Any	Single antenna mode. Only Channel A active. LED 4 green, LED 3 red
MIMO 2×2	Any	Dual channel default. Both channels active. LED 3+4 green

Note: Only one technology mode (4G or 5G) can be active on a single unit at a time. Band selection is performed at service start time. Maximum bandwidth: 20 MHz (TDD), 10 MHz (FDD).

4 Detailed Connector Pin-Outs and Specifications

4.1 4.1 RF Connectors — Electrical Characteristics

The rear panel RF connectors are shown in Figure 4-1. The following table provides detailed electrical specifications:

RF Port Electrical Specifications

Parameter	TRXA/TRXB	RXA/RXB
Connector Type	SMA Female	SMA Female
Characteristic Impedance	50Ω	50 Ω
TDD Function	Bidirectional TX/RX	Not used
FDD Function	TX output	RX input
Max Safe Input	+10 dBm (absolute max, do not exceed)	Same
TX Output Power	+3 dBm modulated (freq dependent)	N/A
TX Noise Figure	N/A	< 2 dB (LNA stage)
VSWR	< 2:1 (with matched antenna)	Same
Frequency Range	30 MHz – 3.8 GHz	Same
DC Blocking	Internal DC block present	Same

The LMS7002M internal T/R switch provides approximately 25 dB of TX-to-RX isolation during TDD operation. For FDD, external duplexers are required between the antenna and the TX/RX ports if a single antenna per channel is desired.

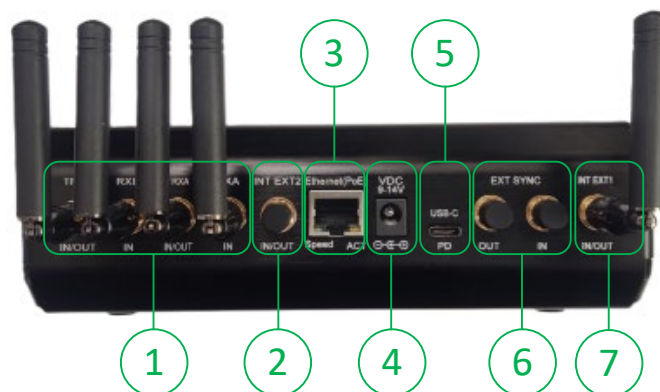


Figure 4-1: Rear panel connector layout. 1: RF ports (TRXB, RXB, TRXA, RXA), 2: INT EXT2, 3: Ethernet PoE, 4: USB-C, 5: DC Power, 6: EXT SYNC, 7: INT EXT1.

4.2 INT EXT2 — GNSS / Configurable Port

INT EXT2 Specifications

Parameter	Specification
Connector	SMA Female
Standard Function	GNSS receiver antenna input
Supported Constellations	GPS (L1), GLONASS (L1), Galileo (E1), BeiDou (B1)
Antenna Type	Active or passive GNSS antenna
DC Bias	Available for active antenna power (check board config)
Customization	Function depends on internal board configuration — can be repurposed

4.3 EXT SYNC — External Synchronization

EXT SYNC Specifications

Parameter	Specification
Connector	SMA Female
Function	External reference clock input for transceiver/FPGA synchronization
Use Case	Multi-unit clock synchronization for MIMO, carrier aggregation
Input Level	Standard CMOS/LVCMOS levels (check gateway documentation)
Reference Frequency	Depends on CDCM6208 configuration
Critical For	Phase-coherent multi-unit operation, distributed MIMO

4.4 DC Power Connector — Engineering Detail

DC Power Specifications

Parameter	Specification
Connector	5.5 mm OD × 2.1 mm ID barrel jack
Polarity	Center positive
Nominal Input	12 V DC
Input Tolerance	±5% (11.4 V – 12.6 V recommended)
Max Current Draw	2.08 A (at 25 W maximum)
Protection	Reverse polarity diode, resettable PTC fuse (over-current)
Inrush Current	< 3 A peak for < 10 ms
Ripple Tolerance	< 200 mV p-p recommended for optimal RF performance

Tip: For best RF performance, use a low-noise, well-regulated power supply. Excessive ripple on the 12V rail can couple into the RF chain and degrade ACPR and EVM.

4.5 USB-C Port — Detailed Functions

USB-C Functions

Parameter	Specification
Primary Function	Alternative power supply delivery (12 V DC via USB-C PD)
Secondary Function	RPi5 Compute Module boot mode entry
Tertiary Function	Firmware update / eMMC flashing via rpiboot
Data Transfer	USB 2.0 speeds when used for boot/firmware
Warning	Do not use simultaneously with DC barrel for power

4.6 GPIO Header — Pin Mapping Considerations

The 40-pin GPIO header follows the standard Raspberry Pi 5 pinout. The side panel connectors are shown in Figure 4-2. However, the M.2 HAT+ adapter for PCIe communication with the LimeSDR XTRX reserves several GPIO pins:

GPIO Usage Notes

Parameter	Specification
3.3 V Power	Pins 1, 17 — 3.3 V supply (limited current available)
5 V Power	Pins 2, 4 — 5 V supply from main rail
Ground	Pins 6, 9, 14, 20, 25, 30, 34, 39 — ground reference

Parameter	Specification
I2C (Bus 1)	GPIO 2 (SDA), GPIO 3 (SCL) — used by HATs, EEPROM
SPI (Bus 0)	GPIO 8-11 — available if not used by PCIe HAT
UART	GPIO 14 (TX), GPIO 15 (RX) — serial console
PCIe Reserved	Specific pins reserved by M.2 HAT+ — consult RPi5 CM docs
PWM	GPIO 12, 13, 18, 19 — available for fan control, etc.

CRITICAL: Always consult the RPi5 Compute Module datasheet and M.2 HAT+ documentation before connecting any custom hardware to GPIO pins. Bus conflicts can cause system instability, data corruption on the PCIe link, or hardware damage.

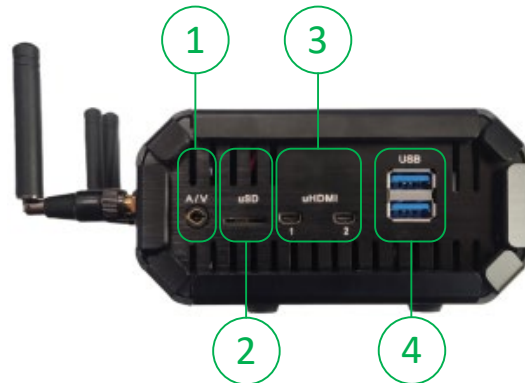


Figure 4-2: Side panel connector layout. 1: Audio 3.5mm TRRS, 2: Micro-SD slot, 3: Micro HDMI 2.0 (2×), 4: USB 3.0 Type-A (2×).

5 Clocking and Timing Architecture

The clock subsystem is one of the most critical aspects of the LimeSDR XTRX design, as precise timing directly impacts RF signal quality, cell synchronization accuracy, and multi-unit coherence.

5.1 Clock Distribution Network

Clock Chain Detail

Parameter	Specification
VCOXO	Voltage-Controlled Crystal Oscillator. Primary ultra-low-phase-noise reference. Output feeds CDCM6208 input
VCTCXO	Temperature-Compensated reference (± 0.2 ppm). Secondary reference, can be GPS-disciplined via DAC control
CDCM6208	TI clock distribution/jitter cleaner IC. Takes reference input and generates: FPGA system clock, LMS7002M reference clock, ADC/DAC sampling clocks, PCIe reference clock
GNSS 1PPS	Pulse-per-second from integrated GNSS receiver. Used to discipline VCTCXO for sub-microsecond timing accuracy
EXT SYNC Input	External SMA input. Accepts external reference for multi-unit synchronization. Bypasses internal oscillators
NTP/PTP	Network-based timing via Ethernet. Provides millisecond (NTP) or microsecond (PTP) synchronization

5.2 Clock Configuration Scenarios

Standalone Single Cell: Internal VCTCXO provides sufficient accuracy (± 0.2 ppm). No external reference needed. GNSS disciplining optional but recommended for best frequency accuracy.

GNSS-Disciplined: Connect a GNSS antenna to INT EXT2. When GPS lock is achieved, the 1PPS signal disciplines the VCTCXO via a control loop, achieving sub-100 ppb frequency accuracy and sub-microsecond timing.

Multi-Unit Synchronized: Connect all units to a common external reference clock via EXT SYNC. This ensures phase-coherent operation across units for MIMO, carrier aggregation, or coordinated multi-point (CoMP) deployments.

Network-Timed: NTP/PTP via Ethernet provides coarse timing synchronization. Suitable for coordinated scheduling but insufficient for phase-coherent MIMO.

6 RF Signal Paths and Configuration

6.1 LMS7002M Internal Architecture

The LMS7002M is a full-duplex, dual-channel FPRF transceiver with integrated LNA, PA driver, mixers, ADC, DAC, and PLL synthesizers. Key internal signal path components:

- TX Chain: Digital interface → DAC → Low-pass filter → Mixer (up-conversion) → PA driver → External matching → SMA connector
- RX Chain: SMA connector → LNA (selectable gain) → Mixer (down-conversion) → TIA → Low-pass filter → PGA → ADC → Digital interface
- PLL Synthesizers: Two independent PLLs (SXT for TX, SXR for RX) provide LO generation for the full 30 MHz – 3.8 GHz range
- T/R Switch: Internal antenna switch for TDD operation (~25 dB isolation)

6.2 TDD Operation Mode

In TDD mode, TRXA and TRXB connectors operate bidirectionally. The internal T/R switch alternates between TX and RX based on the subframe timing from the Amarisoft stack. RXA and RXB ports are not used for signal but should still have antennas or 50Ω loads attached for proper matching.

TDD timing is controlled by the DFE gateway in the Artix-7 FPGA, which generates precise TX/RX switching signals synchronized to the subframe boundary. Maximum bandwidth: 20 MHz.

6.3 FDD Operation Mode

In FDD mode, separate TX and RX paths are used simultaneously. TRXA/TRXB carry TX output, while RXA/RXB receive RX input. Both PLLs (SXT and SXR) run at different frequencies for uplink and downlink.

External duplexers are required if a single antenna per channel is desired (e.g., for Band 7 FDD operation). The duplexer must be selected for the specific band and provide sufficient TX-to-RX isolation. Maximum bandwidth: 10 MHz.

6.4 MIMO vs. SISO Configuration

In MIMO 2×2 mode (default), both channels A and B are active. LED 3 indicates Channel B, LED 4 indicates Channel A. In SISO mode, only Channel A is active (LED 4 green, LED 3 red). SISO mode is configured via the Amarisoft stack configuration file.

For massive MIMO deployments beyond 2×2, multiple LimeSDR XTRX boards (via multiple LimeNET Micro units) can be combined. Each unit provides one 2×2 building block, scalable up to 32T32R with appropriate clock synchronization via EXT SYNC.

6.5 RF Power Control — Detailed Engineering Reference

Two independent gain control mechanisms are available, and they can be combined:

tx_gain [0–50] — Analog Gain: Controls the LMS7002M RF IC transmitter analog gain. Value 50 represents maximum TX power (minimum attenuation). Step size is 1 dB from 50 down to 40, and 2 dB from 40 down to 0. Important: every second step below 40 has no effect (e.g., 40→39 reduces by 2 dB, 39→38 has no change). Channel-selectable.

cell_gain [-200–0] — Digital Gain: Controls the digital gain of the transmitted signal in the DFE. Preferred method for most operational use cases. Value 0 = no attenuation, -200 = maximum attenuation. Does NOT update the SS PBCH block power in SIB1 (cell_gain is applied after SIB encoding). Applies per cell ID.

Runtime adjustment methods:

```
# Remote API (WebSocket)
./ws.js enb '{"message":"rf","tx_gain": 50, "tx_channel_index": 0}'
./ws.js enb '{"message":"cell_gain","cell_id": 1, "gain": -20}'
```

```
# nodeB terminal command line
tx_gain 50 0      # Set analog gain to max on channel 0
cell_gain 1 -20   # Attenuate cell 1 digital signal by 20 dB
```

For permanent power settings, edit the RF driver configuration file in `~/LimeNET/egnb/config/rf_driver/` and set the `tx_gain` parameter. The main config file (`xtrx_LimeNET_*G_***.cfg`) includes the RF driver config.

7 Internal Buses, I/O Mapping, and FPGA Interfaces

7.1 PCIe Interface

PCIe Link Specifications

Parameter	Specification
Generation	PCIe Gen2
Lanes	x1
Bandwidth	5 GT/s (approximately 500 MB/s each direction)
Physical Interface	M.2 HAT+ adapter (RPi5 CM ↔ LimeSDR XTRX)
Kernel Driver	Open-source PCIe kernel module (github.com/myriadrf)
Data Format	IQ sample streams (interleaved I/Q, 12-bit per sample)
DMA	Bus-master DMA for zero-copy sample transfer
Verification	lspci shows LimeSDR XTRX as connected PCIe device

⚠ WARNING: Do not connect other M.2 devices while the LimeSDR XTRX is installed. The M.2 slot is exclusively used for the SDR board.

7.2 SPI Control Bus

The FPGA communicates with the LMS7002M via SPI for register-level control. This bus handles: transceiver configuration and calibration, PLL programming, gain control, filter bandwidth selection, and T/R switch control. The SPI bus operates at several MHz and is transparent to the user — all access is abstracted through LimeSuiteNG library APIs.

7.3 FPGA DFE Block Diagram

The Artix-7 FPGA implements the following signal processing blocks in the Digital Front-End:

- PCIe DMA Engine: Manages high-speed sample transfer to/from host memory
- TX Interpolation Chain: Configurable multi-stage interpolation (x2, x4, x8, x16, x32)
- TX FIR Filter: Programmable 15-tap symmetric FIR for TX pulse shaping
- TX IQ Correction: Phase and amplitude imbalance compensation
- RX Decimation Chain: Configurable multi-stage decimation (matching TX)
- RX FIR Filter: Programmable 15-tap symmetric FIR for RX channel filtering
- RX DC Offset Removal: Automatic DC calibration loop
- RX IQ Correction: Phase and amplitude imbalance compensation
- DPD Engine: Digital Pre-Distortion for external PA linearization
- Timestamp/Sync Logic: Precise sample timing for TDD switching and multi-unit sync
- Clock Management: MMCM/PLL blocks for internal clock domain generation

8 Hardware Revision History and Compatibility

Hardware Revisions

Component	Version	Release / Notes
LimeNET Micro Enclosure	1.0	November 2025 — initial release
BB Carrier Board	1.0	November 2025 — RPi5 CM carrier with M.2 HAT+
LimeSDR XTRX Board	1.3	Current production version
LMS7002M Transceiver	Rev C	Current silicon revision
Artix-7 FPGA	XC7A50T	Standard across all XTRX v1.3 boards
FPGA Gateware	See GitHub	Version tracked per release tag
Technical Guide	1.0	November 2025 (13/11/2025)

Note: Contact Lime Microsystems for detailed ECN (Engineering Change Notice) records and compatibility matrices between hardware revisions, gateware versions, and software releases.

9 Engineering Notes, Caveats, and Best Practices

9.1 Software License Binding — Critical

CRITICAL: The Amarisoft commercial software license is cryptographically bound to the specific Raspberry Pi Compute Module's hardware identifiers: serial number, CPU ID, and MAC address. Transferring the SD card, eMMC image, or software to a different RPi will INVALIDATE the license permanently. If the RPi fails and requires replacement, contact Lime Microsystems support immediately with both the original and replacement serial numbers before installing the replacement.

Record your RPi serial number now and store it securely:

```
cat /proc/cpuinfo | grep Serial
cat /proc/cpuinfo | grep Model
```

9.2 Thermal Design Considerations

- The passive cooling design is rated for 25W at 0–40°C ambient temperature
- CPU thermal throttling begins at 80°C (reduces clock speed to limit temperature)
- CPU thermal shutdown at 85°C (system halts to prevent damage)
- Normal case temperature: 30–50°C (warm to touch is expected)
- Monitor: `vcgencmd measure_temp` — log this value over 24 hours for new installations
- For high-temp or high-load environments, implement active cooling via GPIO PWM fan control
- Never stack units — maintain minimum 10 cm vertical clearance between stacked installations
- Consider thermal compound replacement if unit is field-serviced

9.3 RF Engineering Best Practices

- Maximum modulated TX output: +3 dBm/channel (LMS7002M output stage limit)
- For higher EIRP, add external PA + bandpass filter (custom FEM available from Lime)
- Always connect all antennas before powering on — unterminated TX ports reflect power
- Use 50Ω SMA loads on unused ports if antennas are not connected
- Keep SMA torque to 0.56–0.9 N·m (finger-tight + 1/4 turn) — do not use wrenches
- Cable loss must be factored into link budget — use low-loss RF cables for external antennas
- For FDD operation, always use external duplexers rated for the specific operating band
- ACPR > 45 dB ensures compliance with most regulatory emission masks

9.4 PCIe Interface and Gateware Notes

- Verify PCIe link after every boot: `lspci | grep Lime`

- PCIe kernel driver version MUST match FPGA gateway version — mismatches cause data corruption
- After gateway flash, always reboot and verify with `lspci`
- PCIe DMA uses bus-master mode — other DMA-heavy peripherals may contend for bandwidth
- The M.2 slot is electrically PCIe x1 Gen2 — do not attempt to use M.2 SATA devices

9.5 Storage and Filesystem Notes

- eMMC has finite write endurance (~100K P/E cycles) — minimize unnecessary writes
- Configure syslog to RAM-based tmpfs to reduce eMMC wear
- For extensive logging, use external USB storage or network NFS/CIFS mount
- Monitor free space: `df -h` — keep utilization below 80%
- Micro-SD slot is available for CMs without eMMC (non-standard configuration)

9.6 Network Deployment Engineering

- Use wired Ethernet for production backhaul — Wi-Fi introduces jitter and reduces throughput
- Configure static IP (avoid DHCP lease expiry causing service interruption)
- Enable SSH key-based authentication (disable password auth for production)
- Set up monitoring with SNMP, Prometheus, or custom scripts for unattended operation
- Disable graphical desktop for optimal CPU availability: `sudo systemctl disable lightdm`
- Configure watchdog timer for automatic recovery from software hangs
- Use UPS or PoE with battery backup for power continuity in production deployments
- Backup all configuration files to off-device storage before any changes
- Test every change incrementally — complex multi-parameter changes make debugging difficult

9.7 Multi-Unit Synchronization Engineering

- For phase-coherent multi-unit operation:
- All units must share a common clock reference via EXT SYNC daisy-chain or distribution
- Cable lengths between clock distributor and each unit should be matched (± 1 cm)
- Use phase-matched RF cables for antenna feeds in MIMO configurations
- Verify synchronization by comparing 1PPS outputs across units (oscilloscope)
- The Amarisoft stack supports coordinated scheduling across multiple units via Remote API

End of Document

This concludes the LimeNET Micro 2.0 series Hardware Reference Manual. For additional support, please contact Lime Microsystems.

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